In the Specification

Pursuant to 37 CFR 1.312, Applicant hereby amends the specification:

Please replace the paragraphs below with the following amended paragraphs:

Please replace the paragraph beginning on page 3, line 20 with the following amended paragraph (in line 27, 104 should be 112).

As to the transmit side of the POTS signal path 98, the DSP 118 provides a sampled data stream to a digital filter 122, e.g., an interpolation filter. As with the data out of the decimation filter 116, the sampled data stream into the interpolation filter 122 typically has a sample rate of 7 to 48kHz. Each sample of the sampled data stream typically comprises 16 bit digital data. The interpolation filter 122 outputs a data stream that has higher sample rate than that out of the DSP 118. The data stream is supplied to a DAC 124. The DAC 124 converts the sampled data stream to an analog signal that is supplied to the POTS AFE ~~104~~112, whereby the analog signal is coupled to the isolation barrier 110.

Please replace the paragraph beginning on page 20, line 3 with the following amended paragraph:

As discussed with respect to **Fig.** ~~10A~~10, the communication link 322 of **Fig.** 12A is shown as a phone line that carries a tip/ring signal, and may support POTS and ADSL (and/or other phone line signal protocols). However, the communication link is not limited to such. Furthermore, the illustrated embodiment of the device 360 supports POTS and ADSL, but the device is not limited to such.

Please replace the paragraph beginning on page 24, line 1 with the following amended paragraph:

Fig. 15A has a curve ~~440~~441 that illustrates the magnitude of the termination impedance provided by the termination impedance circuit 426 in the ADSL only state.

Please replace the paragraph beginning on page 24, line 16 with the following amended paragraph:

If on the other hand, the "off-hook" signal indicates an "off-hook" state, then the switch 436 is in the closed state, whereby the termination impedance circuit 426 is the ADSL and POTS state. The graph in **Fig.** 15B has a curve ~~442~~443 that illustrates the magnitude of the termination impedance provided by the termination impedance circuit 426 in the ADSL and POTS state. In the ADSL and POTS state, the combination of the second impedance, e.g. Zt_{POTS}, and the DC blocking component 434, is connected in parallel with the blocking component 430. At frequencies from 50Hz to 552kHz, the termination impedance circuit 426 presents an impedance equal to a sum of the first impedance and the second impedance (e.g., $Zt_{ADSL} + Zt_{POTS}$), which results in an impedance profile that approximately matches that of a typical phone line. At frequencies below 50 Hz the impedance of the DC blocking component 434 preferably becomes large enough to dominate.

Please replace the paragraph beginning on page 32, line 26 with the following amended paragraph:

The ADSL interpolation filter 650 and the POTS interpolation filter ~~650~~652 receive an ADSL sampled data stream and a POTS sampled data stream, respectively. The

ADSL interpolation filter 650 and the POTS interpolation filter 652 each outputs a separate data stream, which are combined 654 into a single data stream. In one embodiment, the input sample rate to the ADSL interpolation filter 650 is 1.104 MHz +/- 400 ppm or 552 KHz +/- 400 ppm, the input sample rate to the POTS interpolation filter 652 is in a range between 7 kHz and 14 kHz, controllable in increments of 1 Hz, and the output sample rate of each of the interpolation filters is 8.192 MHz. In some embodiments, the sample rate out of the ADSL interpolation filter 650 may not be equal to the sample rate out of the POTS interpolation filter 652, however, in such embodiments, it may be desirable to make one of the sample rates an integer multiple of the other of the sample rates.

Please replace the paragraph beginning on page 33, line 18 with the following amended paragraph:

The POTS Receive Decimation Filter 662 has a digital filter 670 that receives the sampled data stream (e.g., having a fixed sample rate of 8.192MHz), via a signal line ~~671~~701, from the ADC. The digital filter 670 outputs a sampled data stream, which is supplied to a decimator 672 having a fixed decimation ratio of 4. The output from the decimator 672 is input to an interpolator 674 having a variable interpolation ratio the value of which is controlled by the POTS Sample Rate control signal. The output of the interpolator 674 is a variable rate data stream, which is input to a digital filter 676 in series with a decimator 678 having a fixed decimation ratio of 1024. The decimator 678 outputs a sampled data stream, which is input to a gain correction block 680. The gain correction block 680 allows the POTS Receive signal level to be controlled by the user and corrects for gain errors that were introduced by the variable interpolation block 674. The output from the gain correction block 680 is supplied to one input (i.e., a POTS Receive Decimation path input) of the Monitor Speaker path 668. The output of the gain correction block 680 is also supplied to a digital filter 682 followed by a decimator 684 having a fixed decimation ratio of 2. The decimator 684 outputs a sampled data stream that is supplied to another digital filter 686 followed by a decimator 688 having a fixed decimation ratio

of 2. The output of the decimator 688 is the POTS Receive data stream having a variable sample rate of 7kHz to 14kHz.

Please replace the paragraph beginning on page 34, line 5 with the following amended paragraph:

The ADSL Receive Decimation Filter 660 has a variable interpolation function 700 that receives the sampled data stream (e.g., having a fixed sample rate of 8.192MHz), via a signal line ~~671~~701, from the ADC. The variable interpolation 700 is controlled by the ADSL Sample Rate control signal. The variable interpolation function 700 outputs a sampled data stream having a variable sample rate, which is supplied to a digital filter 702. The output from the digital filter 702 is supplied to decimator 704 having a fixed decimation ratio. The output of the decimator 704 is supplied to another digital filter function 706 followed by a another decimator 708 having a fixed decimation ratio of 2. The decimator 708 outputs a data stream having a variable sample rate of 2.208MHz +/- 400ppm. This variable sample rate data stream is input to a filter 710 in series with a decimator 712 that decimates by a factor of two to produce a sampled data stream having a variable sample rate of 1.104MHz +/- 400ppm. In this embodiment, either the 1.104MHz +/- 400ppm data stream or the 2.208MHz +/- 400ppm data stream is supplied to the DSP as the ADSL Receive Data Stream.

Please replace the paragraph beginning on page 35, line 4 with the following amended paragraph:

The ADSL Transmit Interpolation Filter 664 has an input that receives a variable sample rate data stream from the DSP. In this embodiment, the variable sample rate data stream has a sample rate of 552kHz +/-400ppm or a sample rate of 1.104MHz +/- 400ppm sample stream . If the sample rate is 552kHz +/-400ppm, the variable rate data stream is input to an interpolator 742, which has a fixed interpolation value of two. The interpolator outputs a data stream, which

is supplied to a digital filter function 744. The output of the digital filter is a data stream having a variable sample rate of 1.104 +/- 400ppm. This data stream is input to an interpolator 746 having a fixed interpolation value of 2. On the other hand, if the sample rate of the variable sample rate data stream from the DSP is 1.104MHz +/- 400ppm, then the variable rate data stream from the DSP is input directly to the interpolator 746, thereby bypassing the interpolator 742 and digital filter 744. The interpolator 746 outputs a sampled data stream that is supplied to a digital filter 748. The output from this filter 748 is input to another interpolator 750 with a fixed interpolation value of 2 in series with a digital filter 752. The output from the digital filter 752 is input to an interpolator 754 having a fixed interpolation value of 2^{23} . The interpolator 754 supplies a digital filter 756, which outputs a data stream having a variable sample rate. The variable sample rate data stream is input to a decimator 758 having a variable decimation ratio. This decimation ratio is controlled by the ADSL Sample Rate control signal. The output from the decimator 758 is a data stream having a fixed sample rate of 2.048MHz, which is input to a Gain block 760 that allows the signal to be adjusted under user control. The output from this gain block 760 is a fixed sample rate representation of the ADSL Transmit signal. This signal is supplied to the summing block 740, which sums the data stream with the 2.048MHz fixed sample rate output from the POTS Interpolation Path. The output from the summing block 740 is input to an interpolator ~~742~~743 with a fixed interpolation ratio of 4. The output from the interpolator ~~742~~743 is input to a digital filter ~~744~~745 the output of which is a data stream having a fixed sample rate of 8.192MHz. This data stream is input to the digital sigma-delta modulator ~~746~~747 to produce the 4-bit DAC data stream having a fixed sample rate of 8.192MHz.

Please replace the paragraph beginning on page 37, line 13 with the following amended paragraph:

The transfer function 840, (**Fig.** 23) of DAC 830 shows DC voltages of 0, 1, 2 and 3 for the digital inputs of 00, 01, 10 and 11. When the simple straight forward implementation of DAC

830 is used a problem can occur because the signal level may remain steady when the particular digital input value remains unchanged for a number of contiguous clock pulses. Thus, if the digital value 01 was transmitted for three or four clock cycles or more, there would be no change in the voltage level and there would be a loss of signal across the capacitor 818 of the isolation barrier which cannot pass or transmit DC levels. The frequency spectrum of DAC 830 appears as shown at 842 (**Fig.** 24) where it can be seen that most of the energy is concentrated at lower frequencies which are blocked by the capacitor. To improve the performance it is desired to have a system that effects the signal transmitted across the isolation barrier so that it has a constant average signal in the nature of a periodic signal so that it passes normally through a capacitive or transformer coupling. One implementation to address this problem is shown in **Fig.** 25 where digital to analog circuit 812b includes an encoder 850 that receives the digital input at 814b and delivers such a constant average signal to the input 852 of DAC 854. A termination resistor 856 has also been added to affect common mode rejection. Since this is a unidirectional embodiment termination resistance 856 is not actually required. Analog to digital circuit 822b includes an analog to digital converter 858 which senses the constant signal average output 820b from isolation barrier 818b, converts it to a digital signal, and delivers it to decoder 862. Decoder 862 then provides the digital output on line 824b. Analog to digital circuit 822b also includes a termination resistance 866 to reduce common mode errors. Common mode rejection or reduction is accomplished because any common mode signal that occurs across resistance ~~836~~856 will be suppressed through resistance 866 and V_{ref} so that the input 820b to ADC 858 can be kept at its proper level. The isolation circuit need not be capacitive. It could as well be a transformer as shown at 818b.

Please replace the paragraph beginning on page 40, line 3 with the following amended paragraph:

In the first instance, common mode rejection is effected through termination resistance 960 and 972. The effect of termination resistors 960 and 972 is to limit the voltage at 982 to a function of the digital voltage at input 990 plus that at input 992 divided by two. This significantly reduces the common mode interference by a factor of two. To further reduce the common mode interference, common mode rejection circuit 1000 may be employed. It consists of an amplifier 1002 and termination resistor 1004 on one side and a similar amplifier ~~206~~1006 and termination resistance ~~208~~1008 on the other side with an isolation capacitor ~~1010~~1011 between them. Amplifiers 1002 and 1006 are driven by a DC common mode signal. Any variation in that common mode signal is sensed at 1010 and 1012 respectively, and delivered to summing circuits 958 and 970, respectively, where they are subtracted from the incoming signal. This further reduces the common mode interference signals beyond what is accomplished by termination resistors 960 and 972 and isolation capacitor 818d.

Please replace the paragraph beginning on page 40, line 16 with the following amended paragraph:

A more detailed embodiment is shown in **Fig.** 31 ~~where as including~~ where are included a number of data channels 1050, 1052, 1054, 1056, 1058 and 1060 for simultaneous bi-directional transmission and reception. Also included are bi-directional control channels 1062 and 1064 and common mode rejection circuit 1000[[a]] as well as ground capacitor 974e. A clock channel is also provided using amplifiers 1070 and 1072 to provide the clock and ~~inverter~~inverter clock signals respectively to a reference amplifier ~~1074~~1076 ~~and clock output capacitor 1076~~. Resistance 1078 and 1080 are termination resistors that are in conjunction with the isolation capacitor 818e again provide common mode rejection or suppression. The isolation barrier is not limited to the embodiments shown in Figs. 21-31. For example, as shown in **Fig.** 32, barrier interface circuit 812f may include a digital to analog converter 1100 which drives a modulator 1102 that provides the constant average signal through isolation barrier 818f to demodulator 1104 whose output is delivered to analog to digital converter 1106 in barrier interface circuit 822f and provides that digital output at 824f. Termination resistors 856f and 866f may be employed again to meet termination requirements and to suppress common mode errors.